

Predictive Current Control for Voltage Source Inverters Considering Dead-Time Effect

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Abstract—This paper proposes a new concept of synthesized voltage vector to address dead-time effect issue for Finite Control Set Model Predictive Control (FCS-MPC) technique. For a voltage source inverter (VSI), dead-time is inevitably inserted between the turn off and turn on instants of power devices to avoid short circuit phenomenon. The influence of dead-time leads to output voltage vector error of three-phase inverters. Furthermore, it will result in computing deviation in cost function, and will deteriorate the performance of the system if not properly dealt with. In this paper, the problem is clearly analyzed, and the solution to this issue is proposed by introducing a synthesized voltage vector. The proposed solution is verified by Hardware-in-the-loop (HiL) test in real time, and results validate the effectiveness of the proposed solution.

Index Terms—Dead-time, model predictive control, voltage source inverter.

I. INTRODUCTION

IN the past decades, Finite Control Set Model Predictive Control (FCS-MPC) has attracted considerable attention in power electronics and electrical drives. Its effectiveness has been proved by various power converter topologies and applications [1]–[4], [21], [22]. FCS-MPC explores the discrete attribute of power converters and uses a fixed sampling time to update the control sequence, therefore, pulse width modulator is not required. It predicts the future behavior of the system with finite control set for the given horizon. Then the switching sequence which minimizes the predefined cost function is selected, and its first element is applied [5], [6]. This process will be repeated when new measurements are updated at the beginning of a new sampling interval.

Predictive current control has been well reported in previous literature in applications of grid connected converter [1], electrical drives [5], and uninterruptible power supply [7]. The main research topics in this domain include but not limited to computational efficiently FCS-MPC, long horizon MPC, fixed

switching frequency MPC and centralized MPC. A brief introduction about the state of the art of these research topics are given in the following.

In [8], an effective two-step method is proposed to reduce the computational burden without deteriorating steady state and transient control performance. On the other hand, it has been proved that long horizon MPC can improve the static performance and system stability. In [9] and [10], long horizon MPC is adopted in power converters. The geometrical structure of the underlying optimization problem is exploited, and an efficient optimization algorithm, called sphere decoding algorithm, is derived.

One natural disadvantage of MPC on control of power converters is that the switching frequency is not a fixed value. This will bring inconvenience to the design of passive filters. A fixed switching frequency scheme for FCS-MPC is presented in [11]. The output waveform quality that compares well to that of a PWM based linear controller. Meanwhile, the merits of FCS-MPC, such as fast dynamics and easy to include constraints, are retained. As mentioned above, centralized MPC also draws considerable attention in recent years. By fully exploring the multiple objectives optimization capability of MPC, centralized MPC takes all control objectives into a unified cost function. In [12], for an active front end PWM rectifier, both dc bus voltage and power are included in a cost function using weighting factors. The main advantage of centralized MPC lies in its fast dynamics performance and convenient for implementation.

Dead-time will be inevitably inserted in the transition of power switches in bridge type circuit, such as half bridge, H bridge and three phase full bridge, to avoid short circuit operation. Different methods have been proposed to compensate the effects of dead-time in PWM modulator based control schemes [13]–[15]. However, to the best knowledge of the authors, its negative influence in FCS-MPC has not been discussed in the published literature. Although FCS-MPC has strong robustness to dead-time effect, it is still desirable to clarify the mechanism of dead-time effect. In high switching frequency application, such as SiC or GaN device based power converters, its effect becomes significant.

In this work, phase current control of a three-phase 2-level VSI is used as a case study due to its straightforward structure and widespread application in industry field. The proposed method is easy to extend to other power converter topologies. The problem of voltage-second deviation during one switching period arises due to the dead-time effect, and the predictions of the system behavior, consequently, are inaccurate. Furthermore, the computation accuracy of the cost function is unavoidable

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affected. In this case, the selected switching position is not necessarily the optimal one.

To overcome the adverse effect of dead-time on system performance, a synthesized voltage vector is proposed in this work. Cost function is evaluated using the synthesized voltage vector to eliminate the dead-time effect. The main contributions of this paper are collected as follows:

(i) The dead-time effect on FCS-MPC controlled VSI is analyzed in depth;

(ii) A vector-based voltage deviation term is derived, and modified FCS-MPC with vector-based error compensation is proposed;

(iii) A comparison study focusing on system static performance is implemented with simulation data.

This paper is structured as follows: Section II illustrate the system modeling and description. Section III analyses the dead-time effect with FCS-MPC control. In Section IV, the modified FCS-MPC scheme, based on synthesized voltage vector, is presented. Section V depicts the comparative results and their analysis. Lastly, Section VI concludes this work.

II. SYSTEM MODELING

A balanced R - L - E load is connected to the output of a three-phase 2-level VSI, and a voltage DC source is provided for dc-link. As shown in Fig. 1, the gate signals of the upper switches are defined as S_a, S_b, S_c , and $\bar{S}_a, \bar{S}_b, \bar{S}_c$ for the lower ones assuming the upper and lower switches are operating in complementary mode. Let the integer variable $u_x \in \{0,1\}$ denote the switching position in each leg, where $x \in \{a,b,c\}$. Consequently, there are $2^3 = 8$ admissible switching states in total, and the control set can be described as

$$\vec{u} \in (u_a, u_b, u_c)^T \in \mathcal{U}_8 \triangleq \{000, 001, \dots, 111\}. \quad (1)$$

The pole voltage defined as the voltage potential between the phase leg terminal and negative dc-link, can be obtained as $v_{xN} = u_x V_{dc}$. Therefore, voltage vectors of a VSI can be defined as

$$\vec{v} = \frac{2}{3} \left(v_{aN} + e^{j\frac{2\pi}{3}} v_{bN} + e^{j\frac{4\pi}{3}} v_{cN} \right). \quad (2)$$

By investigating the admissible switching states, eight voltage vectors and corresponding voltage vector index are obtained, which are depicted in Fig. 2.

According to Kirchhoff voltage law, the voltage function of each phase can be obtained

$$v_{xN} = L \frac{di_x}{dt} + Ri_x + e_x. \quad (3)$$

where $x \in \{a,b,c\}$. By invoking (power invariable) Clark Transformation (see (4a)) and Euler Forward method (see (4b)), a discrete-time model of VSI with R - L - E load is derived in $\alpha\beta$ -frame (see (4c))

$$\vec{y}_{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \vec{y}_{abc}, \quad (4a)$$

$$\frac{dy(t)}{dt} = \frac{y(k+1) - y(k)}{T_s}, \quad (4b)$$

$$\vec{i}_{\alpha\beta}^p(k+1) = \left(1 - \frac{RT_s}{L}\right) \vec{i}_{\alpha\beta}^p(k) + \frac{T_s}{L} (\vec{v}(k) - \vec{e}(k)). \quad (4c)$$

Where $\vec{y}_{\alpha\beta}$ represents a variable vector in $\alpha\beta$ -frame, and \vec{y}_{abc} denotes a variable vector in abc -frame. $y(t)$ is a value function of time t . T_s is the sampling time. $\vec{i}_{\alpha\beta} = (i_\alpha, i_\beta)^T$ denotes the measurement of current vector, $\vec{i}_{\alpha\beta}^p = (i_\alpha^p, i_\beta^p)^T$ represents the prediction of current vector, $\vec{v} = (v_\alpha, v_\beta)^T$ corresponds to the inverter output voltage space vector, and $\vec{e} = (e_\alpha, e_\beta)^T$ denotes the load back-EMF.

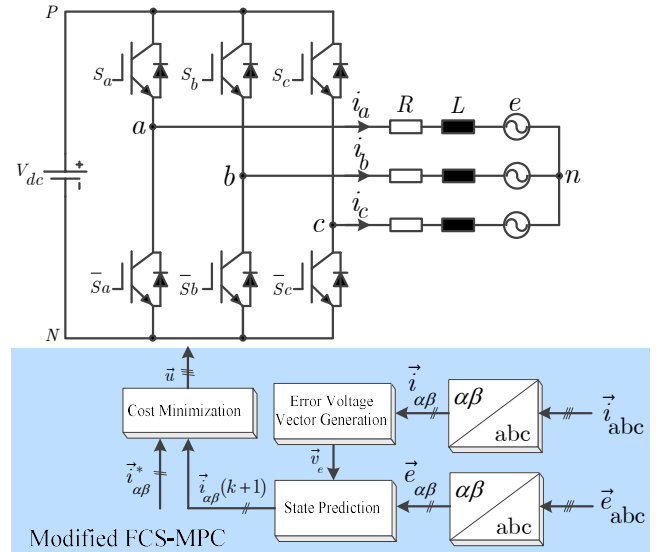


Fig. 1. A Three phase 2-level VSI. S_a, S_b and S_c , present the upper switches, while \bar{S}_a, \bar{S}_b and \bar{S}_c denote for the lower ones.

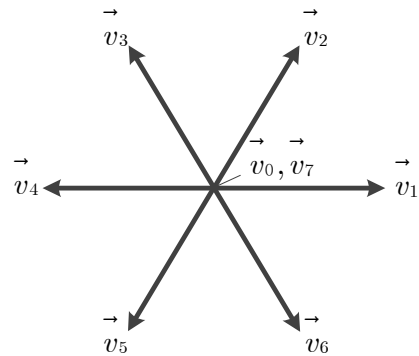


Fig. 2. Voltage vectors depicted in $\alpha\beta$ -frame. There are eight admissible voltage vectors in total: two zero voltage vectors and six active voltage vectors.

III. DEAD-TIME EFFECT ANALYSIS FOR FCS-MPC

Despite many factors, such as turn-on time, turn-off time, and voltage drop on power devices, affect the system performance, the dead-time effect has the most significant influence. In FCS-MPC, despite the effect of dead-time is similar with linear control law with PWM modulator, unique features should be addressed. Fig. 3 shows one leg of a VSI with different current polarity. The switching position, pole voltage and pole voltage error are shown in Fig. 4.

For a specific phase $x \in \{a, b, c\}$ with positive current, assume the previous switching position u_x is 0, and transforms to 1. Dead-time is inserted between the turn off and turn on instant. During dead-time interval, both power switches are in *OFF* state, and the load current flows through freewheeling diode of the lower switch, and pole voltage is clamped to zero volts. In this case, the effective time duration of pole voltage V_{dc} reduces to $(T_s - T_{db})$ instead of T_s , where T_{db} is dead-time interval. Similarly, conclusion can be drawn that pole voltage error will not be introduced when the transition of u_x happens from 1 to 0.

According to voltage second balance principle, the equivalent pole voltage error during one switching cycle is obtained

$$v_{exN} = K_{xcp} \frac{T_{db}}{T_s} V_{dc}. \quad (4)$$

Where $K_{xcp} \in \{-1, 0, 1\}$ is a coefficient determined by the current polarity. Identical analysis method is applicable to the phase leg with negative current as depicted in Fig. 3. The relationship between the pole voltage error v_{exN} and current polarity can be summarized in Table I.

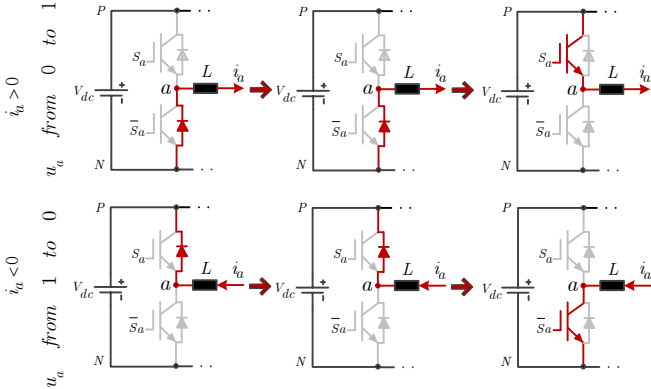


Fig. 3. Dead-time effect with different current polarity: the phase current path during switching transition.

So far, the dead-time effect to the phase pole voltage is carefully studied. To apply the voltage error to FCS-MPC conveniently, some mathematical manipulations are required. Invoking the concept of output voltage vector of inverter in (2), *error voltage vector* is introduced as following:

$$\vec{v}_e = \frac{2}{3} \left(v_{eaN} + e^{j\frac{2\pi}{3}} v_{ebN} + e^{j\frac{4\pi}{3}} v_{ecN} \right) \quad (5)$$

TABLE I
POLE VOLTAGE ERROR VS CURRENT POLARITY

Switching Transition	Current polarity factor	
	$i_x > 0$	$i_x < 0$
$u_x : 0 \rightarrow 1$	$K_{xcp} = -1$	$K_{xcp} = 0$
$u_x : 1 \rightarrow 0$	$K_{xcp} = 0$	$K_{xcp} = 1$
$u_x : 0 \rightarrow 0$	$K_{xcp} = 0$	$K_{xcp} = 0$
$u_x : 1 \rightarrow 1$	$K_{xcp} = 0$	$K_{xcp} = 0$

In the following section, this error voltage vector will be used to formulate a synthesized voltage vector. In this way, a modified FCS-MPC will be proposed taking the dead-time effect into account.

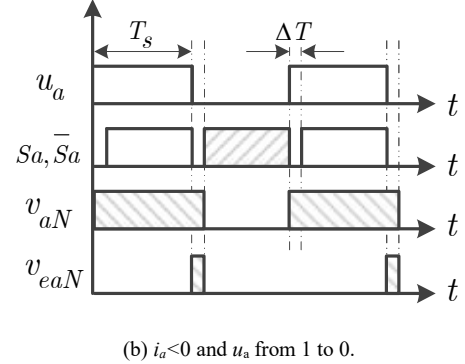
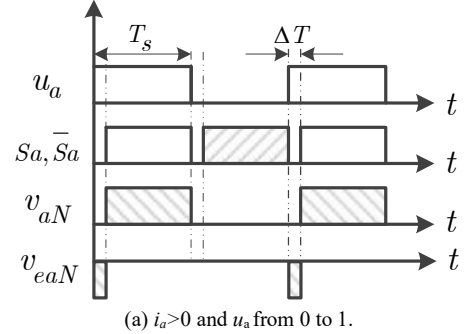


Fig. 4. Dead-time effect with different current polarity. From top to bottom: original switching position, gate signals with dead-time, pole voltage, pole voltage error, respectively.

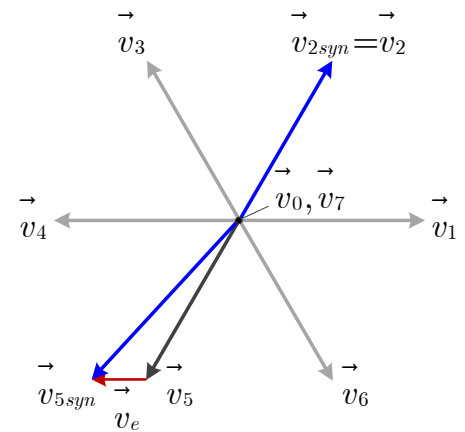


Fig. 5. Voltage vectors depicted in $\alpha\beta$ -frame. The synthesized voltage vector considering the dead-time effect is illustrated.

IV. MODIFIED FCS-MPC CURRENT CONTROL

A. Synthesized Voltage Vector

To solve the fore mentioned problem caused by dead-time effect, this paper proposes a modified FCS-MPC current control algorithm. As shown in (4), the output voltage error can be depicted in a vector form. A synthesized voltage vector can be obtained by combining supposed voltage vector and the error voltage vector (see Fig. 5)

$$\vec{v}_{syn} = \vec{v} + \vec{v}_e. \quad (6)$$

The synthesized voltage vector \vec{v}_{syn} is the actual voltage vector applied to the inverter, and will be used to predict the system behavior. In this way, the predictions gain better accuracy compared to the classical method.

Without loss of generality, at random time instant k and $k+1$, examples of synthesized voltage space vector are illustrated in Fig. 6. Two specific cases are studied, i.e., $\vec{u} : (001) \rightarrow (011)$ and $\vec{u} : (011) \rightarrow (100)$. In the first case, K_{xcp} can be determined using Tab. I since the current polarity is known as: $K_{acp} = 0$, $K_{bcp} = 0$ and $K_{ccp} = 0$. Consequently, there is no prediction error generated in this case, i.e., $\vec{v}_{syn} = \vec{v}$. In the second case, similarly, K_{xcp} can be determined using Table I, $K_{acp} = -1$, $K_{bcp} = 1$ and $K_{ccp} = 1$. According to (2), an error voltage vector $\vec{v}_e = -4T_{db} / 3T * V_{dc}$ is generated, the corresponding synthesized voltage vector is shifted away from the supposed one \vec{v}_s .

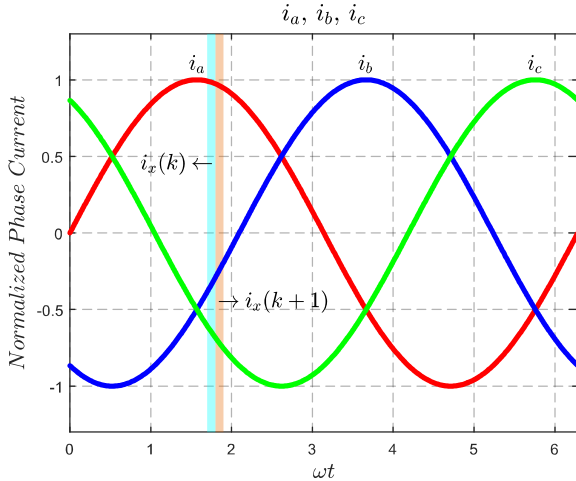


Fig. 6. Error voltage vector with different current polarity: an illustrative example of phase current polarity at time instant k and $(k+1)$.

B. Modified FCS-MPC

In this section, a modified FCS-MPC current control is proposed taking the dead-time effect into account. Instead of compensating error voltage induced by dead-time, synthesized voltage vector is used to predict control variables. Therefore, more accurate predictions are obtained. The proposed control algorithm compensates the time delay as well, using the method

introduced in [16]. Therefore, the modified FCS-MPC is summarized as follows:

ALGORITHM: MODIFIED FCS-MPC

- STEP I:** Update new measurements, and predict control variables at $(k+1)$ time instant to compensate one step time delay.
 - STEP II:** Find out the error voltage vector based on the current polarity and previous switching state using (5).
 - STEP III:** Synthesize the modified voltage vector using (6).
 - STEP IV:** Predict the control variables at $(k+2)$ time instant for all the admissible synthesized voltage vectors.
 - STEP V:** Compute the predefined cost function for all switching combinations.
 - STEP VI:** Select the switching state that minimizes the cost function, and apply the corresponding switching position to the inverter.
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At the next sampling step, the above procedure is repeated. The control variable predictions are obtained using (4c). Cost function is defined as:

$$g = \left(i_{\alpha}^* - i_{\alpha}^p(k+2) \right)^2 + \left(i_{\beta}^* - i_{\beta}^p(k+2) \right)^2. \quad (7)$$

It consists of two terms. The first term penalizes the predicted deviation of the α -axis current from its reference at time step $k+2$. Accordingly, the second term penalizes the β -axis current. For both term, the squared 2-norm is used to formulate the cost function. Since i_{α} and i_{β} have the same importance, the weighting factor is selected as 1.

Another important issue need to be mentioned for the implementation of the modified algorithm. Wrong current polarity might be obtained at the zero crossing point due to the current ripple. Through careful observation, it is not difficult to find that the voltage error caused by dead-time only occurs at the beginning of each sampling period. Inspired by this feature, an effective way to reduce this influence is introduced in the following. By setting up the sampling time instant at the beginning of each sampling period, the current polarity during dead-time can be more accurately detected.

V. COMPARISON STUDY WITH SIMULATION DATA

To verify the effectiveness of the proposed algorithm, a comparison study of current reference tracking between classical FCS-MPC and modified FCS-MPC is performed using Hardware-in-the-Loop (HiL) concept simulation data. Due to safety and cost reasons, it is highly desirable to test the controller in certain scenarios with the help of HiL concept. Real-time signal level simulation system, where the power converter, control plant and controller are realized in powerful digital processors. The picture of HiL test bench is shown below.

Delay compensation is implemented in both methods to guarantee a fair comparison. The simulation scenario is as follows: a VSI inverter is connected to power grid with an L filter which is equivalent to R - L - E load. The fundamental frequency of the grid is 50Hz and the current reference is set at 31A peak value. To ensure the system has settled into steady state, the simulation date is collected after several fundamental periods. DC bus voltage V_{dc} is 800 V, Back-EMF e is 220Vrms, load resistance R is 10 m Ω and load inductance L is 3mH, respectively.

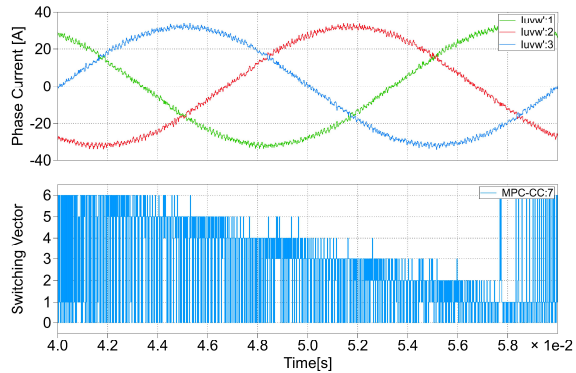


Fig. 7. Hardware-in-the-loop test platform.

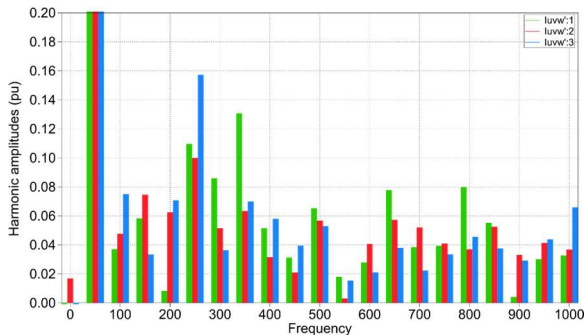
A. Comparison Under 50kHz, 2μs Dead-time

In Fig. 8(a), three phase current and voltage vector index (defined as the subscript of voltage vector) under 50 kHz sampling frequency, 2μs dead-time operating condition are illustrated using classical FCS-MPC. The corresponding spectrum of the phase A current is depicted in Fig. 8(b). The simulation data of modified FCS-MPC under identical scenario is collected in Fig. 9.

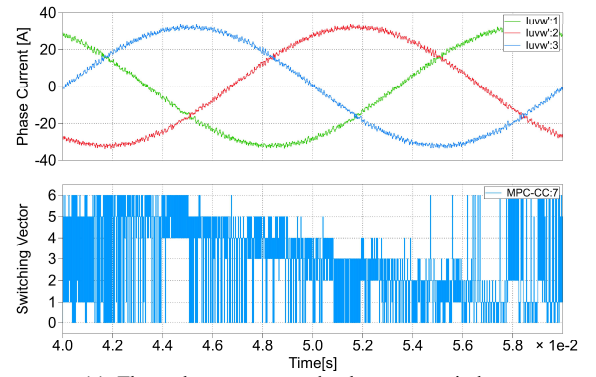
Compared with classical FCS-MPC, the proposed method obtains better static current tracking performance, i.e., lower THD of phase current. Voltage vector index also has significant difference with each other. It proves that the modified method selects optimal voltage vector when taken dead-time into account, however, the classical method might select the suboptimal one. This is in perfect agreement with the dead-time effect analysis in Section III.



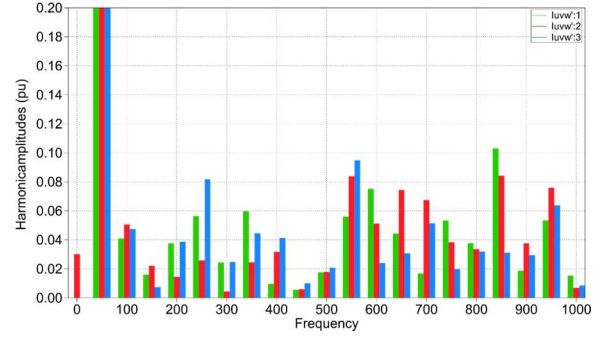
(a) Three phase current and voltage vector index.



(b) Current spectrum.

Fig. 8. Classical FCS-MPC (without considering dead-time effect): operating at $f_{sw}=50\text{kHz}$, $T_{db} = 2\mu\text{s}$.

(a) Three phase current and voltage vector index.



(b) Current spectrum.

Fig. 9. Modified FCS-MPC (considering dead-time effect): operating at $f_{sw} = 50\text{kHz}$, $T_{db} = 2\mu\text{s}$.

From the current spectrum, the maximum of 20th order harmonics are observed. In fact, the harmonics distribution of phase current is strictly below 25 kHz. This fits the fact that the switching frequency is strictly below half of sampling frequency when FCS-MPC is adopted. It is also clear to observe that the current spectrum distribution is relatively even. This is because FCS-MPC has variable switching frequency.

The comparison between classical FCS-MPC and modified FCS-MPC is also conducted. The results show that both method achieve low total harmonic distortion about 3.5%. The classical FCS-MPC shows its robustness against dead-time effect. More specifically, by adopting the proposed modified FCS-MPC, the current THD reduces from 3.79% to 3.49%, and the current quality improvement is 8.6%. This result confirms the effectiveness of proposed method.

B. Comparison Under 100kHz, 2μs Dead-time

With the rapid development of wide band gap devices, such as SiC MOSFETs[17], [18] and GaN HEMTs[19], [20], higher switching frequency is preferred to shrink system volume and weight in high power density applications, such as electrical vehicle and electric aircraft. To evaluate the dead-time effect with different sampling frequency, the same simulation scenario under 100 kHz sampling frequency is carried out and the system performance is evaluated in the steady state.

The simulation data is illustrated in Fig. 10 and Fig. 11 for classical and modified scheme, respectively. Under this test scenario, the phase current THD reduces from 2.52% to 2.02% with adopting the proposed modified FCS-MPC. The improvement of current quality is even more remarkable

compared to the test under 50 kHz, reaching 24.7%. Based on the above analysis, a conclusion can be drawn that the dead-time takes more weight with the increase of sampling frequency. Consequently, the dead-time negative effect is becoming more significant if it is ignored.

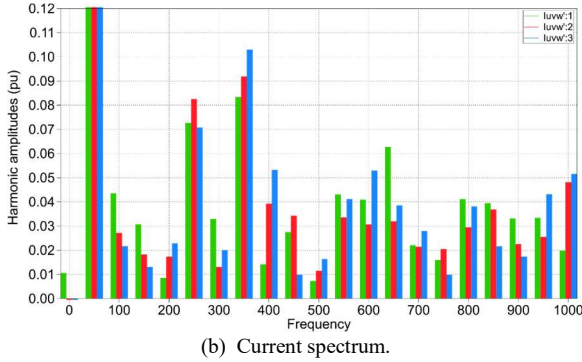
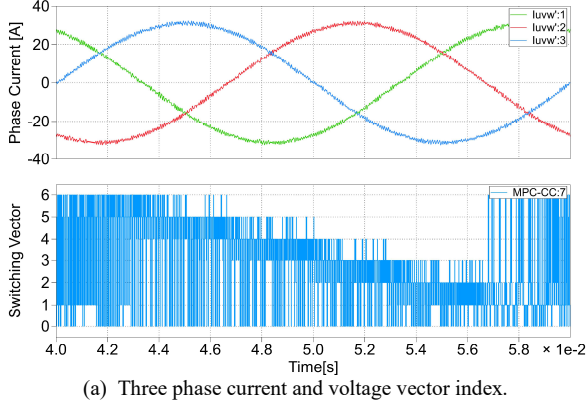


Fig. 10. Classical FCS-MPC (without considering dead-time effect): operating at $f_{sw} = 100\text{kHz}$, $T_{db} = 2\mu\text{s}$.

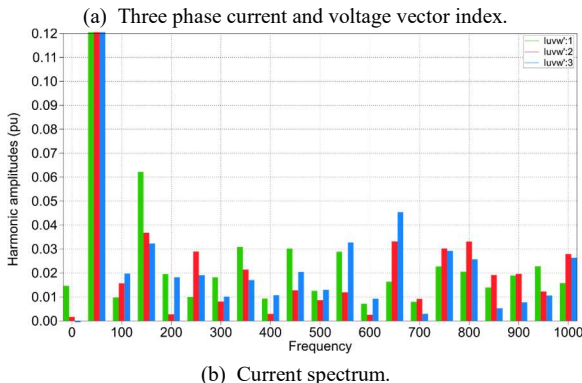
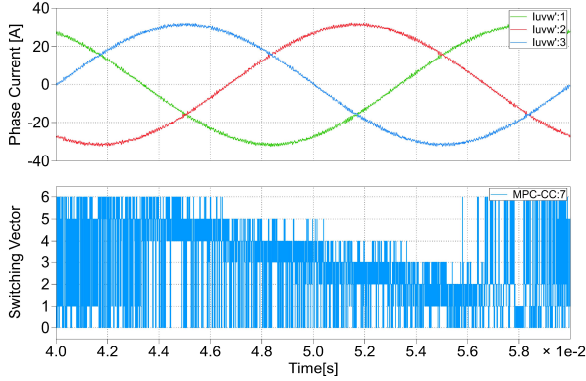


Fig. 11. Modified FCS-MPC (considering dead-time effect): operating at $f_{sw}=100\text{kHz}$, $T_{db}=2\mu\text{s}$.

C. Transient Performance

To further evaluate effectiveness of the modified algorithm, the transient behavior of the system is tested. At the time instant of 0.03 [s], the reference current steps from 15.5 [A] peak value to 31 [A] peak value. The results have been illustrated with 20 μs and 10 μs sampling time in Fig. 11, respectively.

As shown in Fig. 11, the phase current tracks its reference quickly. This result proves that the modified FCS-MPC reserves good dynamic response of classical FCS-MPC. In fact, FCS-MPC manipulates the power switches directly, and apply the optimal switching state to the control plant. By adopting this operational mechanism, cascaded control loops are removed. The modified algorithm does not change the basic control structure of FCS-MPC, therefore, the merits of fast dynamic response is retained.

D. Performance Analysis

As illustrated in the simulation data, FCS-MPC shows it considerable robustness against dead-time effect. Even without considering the dead-time effect, good steady performances are achieved under 50 [kHz] and 100 [kHz] sampling frequency. However, the steady performance is deteriorated as the dead-time becomes significant compared to sampling period.

In fact, the error voltage vector caused by dead-time can be predicted according to the previous switching state and current polarity. Based on the detected error voltage vector, the more accurate synthesized voltage vector is used to predict the system behavior. The modified FCS-MPC with the consideration of dead-time effect improves the steady state performance. Meanwhile, the proposed method inherits the features of FCS-MPC, such as simple and intuitive in concept, ease of including constraints and very fast dynamic response.

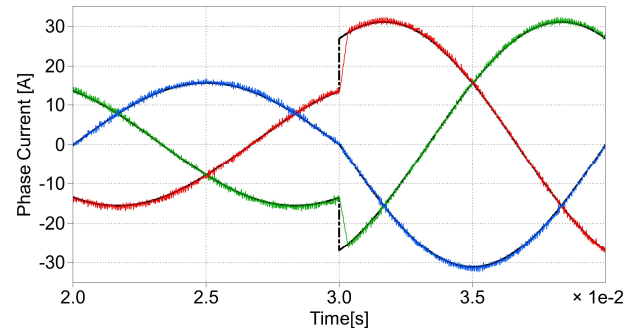
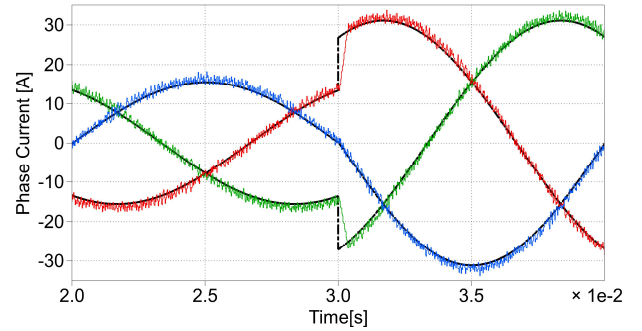


Fig. 12. HiL test results for a step change in the reference current for modified FCS-MPC.

VI. CONCLUSION

In this paper, a new concept of synthesized voltage vector to address dead-time effect when using FCS-MPC has been introduced. The dead-time effect in a VSI is analyzed, and the unique features of this effect in FCS-MPC are presented in detail. The proposed synthesized voltage vector considering the dead-time is generated and used for variables prediction. In this way, the control input voltage vector is more accurately modeled. Consequently, the variables prediction is more reliable, which improves the final current control quality in terms of THDs. HiL simulation data illustrates the effectiveness of the proposed modified FCS-MPC.

The proposed method can be extended to other topologies, such as 3-level T-type inverter and 3-level neutral-point clamped converter. Future work will focus on its application extension.

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